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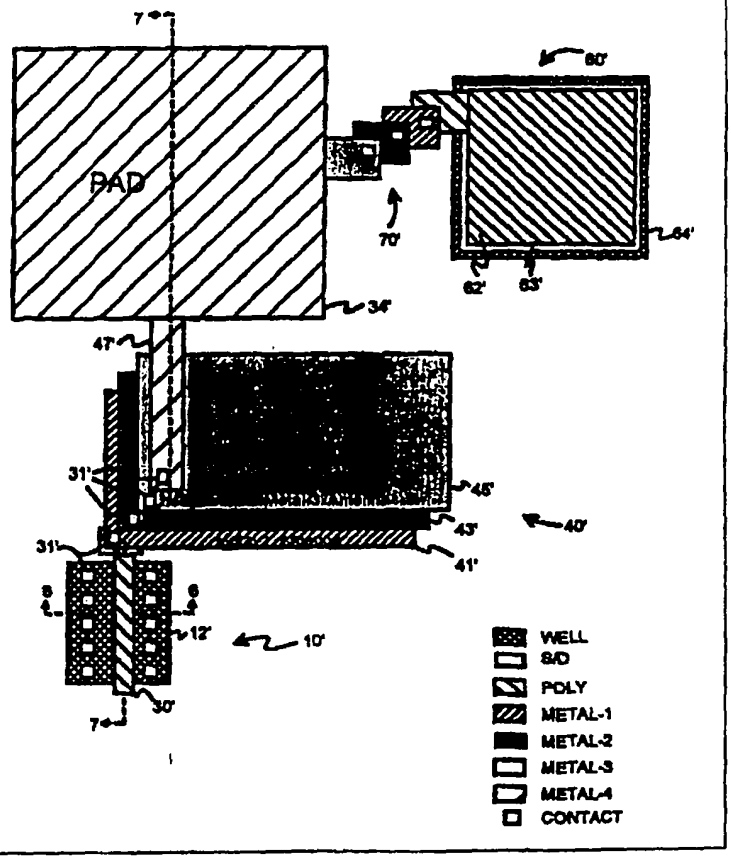
(54) Title: TRANSISTOR STRUCTURE WITH SPECIFIC GATE AND PAD AREAS

(57) Abstract

An improved transistor structure. The novel transistor structure includes a substrate (12'), at least one source disposed on the substrate; at least one drain disposed on the substrate; and at least one gate (30') disposed on the substrate between the source and the drain. The gate has a layer of at least partially conductive material of area Ag. The gate is connected to a pad (34') provided by a single or multiple layer of conductive material area Ap. In accordance with the present teachings, a thin gate oxide capacitor (60') of area Ac is connected to the gate pad via single or multiple layer (70') of conductive material. The area of the third layer is selected such that the ratio R of the area of the second layer Ap to the area of the first layer Ag plus the area of the third layer Ac is equal to a predetermined number. The third layer serves to reduce the antenna effect created by the pad and the multiple layers (40') of conductive material between the gate contact and the pad in accordance with the antenna ratio R.



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Transistor structure with sepcific gate and pad areas

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to transistor design, construction and fabrication. More specifically, the present invention relates to the design of complementary metal-oxide semiconductor (CMOS) transistors for optimal hot carrier injection testing of same.

Description of the Related Art:

CMOS transistors are widely used in applications requiring high-speed, low power digital circuits including microprocessors, memory devices and gate arrays. CMOS transistors are typically fabricated by bonding silicon dioxide layers on a silicon substrate. The silicon dioxide layers are selectively etched away with a plasma current to expose the silicon substrate. Exposed silicon on either side of a nonetched area is implanted with ions to create source and drain areas. A conductive layer is deposited on the nonexposed area to create a gate for the transistor. Additional conductive layers are disposed on the source and drain areas to provide electrical connection thereto. The conductive layers are separated by a dielectric material. Multiple layers of conductive material are also disposed elsewhere on the substrate to provide pads for external connection to the transistor. The pads are connected to the transistor by the conductive layers and the interlayer connections therebetween.

The pad, the conductive layers and and the interlayer connections therebetween act as an antenna and attract plasma current during fabrication. The plasma currents tunnel through the weakly bonded silicon dioxide layer into the silicon substrate. This damages the transistor, impedes its operation, and shortens its useful life.

Conventional transistor designs afford limited control over this problem. The prior approach to the problem has been to test for this tunnel-through with a "Hot Carrier Injection" (HCI) test. The HCI test involves an application of a ground connection to the source terminal and the substrate of a transistor while applying a voltage to the gate and drain terminals. If the current through the device drops below a predetermined threshold, failure of the device is indicated.

Unfortunately, the conventional transistor does not accurately simulate actual processing conditions. Accordingly, the test does not predict failure of certain transistors with a high degree of certainty.

Hence, there was a need in the art for a method for improving the reliability of CMOS transistors. Specifically, there was a need in the art for a system and technique for reducing the deleterious effects associated with plasma tunneling in the fabrication of transistors.

The need in the art was addressed by U. S. Patent Application entitled HOT CARRIER INJECTION TEST STRUCTURE AND TESTING TECHNIQUE FOR STATISTICAL EVALUATION, serial no. _____, filed _____, by N. Bui, the teachings of which are incorporated herein by reference. However, there are certain practical limitations associated with the use of the Bui invention for individual CMOS devices. Individual CMOS devices are generally subjected to a number of tests in addition to those discussed in the Bui application. Some of these tests require that the source, gate and/or drain terminals be accessible and in some cases isolated from the terminals of other devices. Terminal isolation in the above-mentioned device may be impractical and expensive.

Thus, a need remains in the art for a system and technique for reducing the deleterious effects associated with plasma tunneling in the fabrication of transistors which is practical for the fabrication of devices suitable for applications other than testing applications per se.

SUMMARY OF THE INVENTION

The need in the art is addressed by the present invention which provides an improved transistor structure. The novel transistor structure includes a substrate, at

least one source disposed on the substrate; at least one drain disposed on the substrate; and at least one gate disposed on the substrate between the source and the drain. The gate has a layer of at least partially conductive material of area A_g. The gate is connected to a pad provided by a single or multiple layer of conductive material of area A_p. In accordance with the present teachings, a thin gate oxide capacitor of area A_c is connected to the gate pad via single or multiple layers of conductive material. The area of the capacitor is selected such that the ratio R of the area of the gate pad A_p to the area of the transistor gate A_g plus the area of the capacitor A_c is equal to a predetermined number. The gate oxide capacitor serves to reduce the antenna effect created by the pad and the multiple layers of conductive material between the gate contact and the pad in accordance with the antenna ratio R.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an illustrative side view of a die such as that used to fabricate transistors in accordance with conventional teachings.

Fig. 2 is a side view of the die of Fig. 1 with portions of the silicon-dioxide layer thereof etched away to expose the silicon substrate and the doped junctions thereof.

Fig. 3 is a side view of the die of Fig. 2 with a metallization pattern applied to the source, gate and drain terminals thereof.

Fig. 4 is a topological view of the transistor die of Fig. 3.

Fig. 5 is a topological multilayer view of the transistor die of the present invention.

Fig. 6 is a sectional front view of the multilayer die structure of Fig. 5.

Fig. 7 is a sectional side view of the multilayer die structure of Fig. 5.

DESCRIPTION OF THE INVENTION

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Figs. 1, 2 and 3 are illustrative side views of a die such as that used to fabricate transistors in accordance with conventional teachings. The die 10 includes a substrate (typically silicon) on which a layer of material (e.g., silicon-dioxide) 14 is disposed. As illustrated in Fig. 2, the silicon-dioxide layer 14 is selectively removed to create areas 18 and 20 of exposed substrate. One currently favored technique for removing the silicon dioxide layer is to etch the layer 14 with a plasma current. As discussed herein, the plasma current often collects on the gate terminal and tunnels through the silicon-dioxide layer 14. This impairs the operation of the device 10 and limits its life.

The exposed areas 18 and 20 are bombarded with ions to implant impurities and thereby create junctions 22 and 24, respectively. Next, as illustrated in Fig. 3, a metalization pattern is laid down on the exposed areas 18 and 20 as well as the area therebetween to create a source contact 26, a drain contact 28 and gate finger 30 (typically constructed of polysilicon or other suitable material).

Fig. 4 is a top view of the die 10. As illustrated in Fig. 4, the source, gate and drain contacts 26, 30, and 28, respectively, are connected to pads 32, 34 and 36, respectively, by multilayer stacks of conductive material 38, 40 and 42, respectively.

The extent to which the plasma current collects on the gate terminal 30 is determined by the antenna ratio R of the device. The antenna ratio R is given by the relation:

$$R = A_p/A_g \qquad [1]$$

where A_p is the area of the gate pad 34 and the multiple layers of conductive material 40 and A_g is the area of the gate 30.

In accordance with the teachings of the present invention, a polysilicon on silicon dioxide capacitor which connects to the gate pad by a single or multiple layer of conductive material is added for the sole purpose of reducing the antenna ratio R for the last layer of metallization..

Fig. 5 is a topological multilayer view of the transistor structure of the present invention. The structure 10' includes a gate finger 30' on a substrate 12'. Interlayer contacts 31' are provided on both sides of the gate finger 30'. The gate finger 30' is connected to the pad 34' by an arrangement of conductive layers 40'. The multiple conductive layer arrangement 40' comprises first, second, third and fourth layers of metallization 41', 43', 45' and 47', respectively. The first, second, third and fourth layers are interconnected at the interlayer contacts 31' by conductive plugs 35' (not shown). The conductive plugs 35' may be constructed of tungsten or other suitable material. As illustrated in Figs. 6 and 7 below, the plugs 35' extend vertically through dielectric layers into the paper. A pad 34' is connected to the fourth conductive layer 47'. Any conductive layer constructed before the last layer of metallization must satisfy the antenna design constraints. The fourth layer 47' represents a conductive layer which is permitted by the design rules of the structure, but it violates the antenna design constraints.

In accordance with the present teachings, as shown in Fig. 5, the inventive structure includes an additional thin gate oxide capacitor 60'. The capacitor 60' may be fabricated by depositing a layer of polysilicon 62' or other suitable conductive material over a layer of silicon dioxide 63' or other suitable dielectric material on a well 64' (not shown) in the substrate 12. The additional thin gate oxide capacitor 60' is added for the sole purpose of reducing the antenna ratio R. The area of the capacitor 60' is chosen so that when added to the area of the gate, the antenna ratio at the pad layer level R may be estimated by:

$$R = A_p/A_g+A_c \qquad [2]$$

In practice, area of the capacitor 60' A_C should be chosen within the design rules of the structure to lower the antenna ratio within design constraints.

In the multilayer structure of Fig. 5, the capacitor 60' is connected to the pad by a second arrangement of layers of conductive material 70'. The second arrangement

is constructed in the same manner as the first arrangement of layers of conductive material 40'.

Fig. 6 is a sectional front view of the multilayer structure of Fig. 5.

Fig. 7 is a sectional side view of the multilayer structure of Fig. 5.

In Figs. 6 and 7, the gate 30' is shown over the gate oxide layer 14' between the doped junctions 22' and 24' between insulating field oxide layers 53'. An interlayer plug 35' connects the gate finger 30' to the first layer of metallization 41'. As mentioned above, the multiple conductive layers 41', 43', 45' and 47' are interconnected by plugs 35'.

It will be apparent to one skilled in the art that the pad 34', the plugs 35' and the multiple conductive layers 41', 43' and 45' and 47' create an antenna structure. As discussed above this antenna structure attracts plasma current which collects charge at the gate finger 30'. If sufficiently high, this charge may tunnel through the gate xide 14' into the silicon substrate 12' and impair the performance of the structure. The present invention provides a structure in which the antenna ratio is reduced by connecting a capacitor to the pad.

The capacitor 60' is shown with a poly-silicon layer 62' over a silicon-dioxide layer 63'. The poly-silicon layer 62' and the silicon dioxide layer 63' are deposited over a well 64' in the substrate 12'. The transistor die structure 10' is topped by the dielectric oxide layer 49' and a nitride layer 55' for scratch and moisture protection.

As best illustrated in Fig. 7, the pad 34' is in electrical contact with the third conductive layer 45'. The capacitor 60' is in electrical contact with the pad 34' via the multilayer stack 70'. The stack 70' includes plural layers of conductive material 71', 73' and 75' interconnected by interlayer plugs 35'. The capacitor should be located inside a different well relative to the well of the device to which it is connected. This allows the gate current to be measured without the effect of the tunneling current which is drawn to the capacitor. In addition, the charge pumping current measurement will not be substantially affected by the tunneling current at the capacitor 60'. Note also that the distribution of the tunneling current under the capacitor 60' is dependent on the extent to which the oxide thickness is uniform under the poly-silicon capacitor.

Thus, the present invention has been described herein with reference t a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof. The invention may be

implemented with a single layer design or a multilayer design. In any case, antenna ratio between any two layers should satisfy the design rule for any given technology. This design rule is typically the worst case for the antenna design rule to be used in a hot carrier injection test or in a final product.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

WHAT IS CLAIMED IS:

CLAIMS

1. A transistor structure comprising:

a substrate;

at least one source disposed on said substrate;

at least one drain disposed on said substrate;

at least one gate disposed on said substrate between said source and said drain, said gate having a first layer of at least partially conductive material of area A_g;

a second layer of conductive material of area A_p connected to said gate; and

a third layer of conductive material of area A_c connected to said second layer of conductive material, wherein the ratio R of A_p to A_g plus A_c is equal to a predetermined number.

PRIOR ART

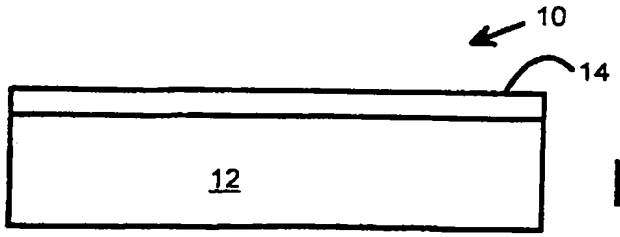


FIGURE 1

PRIOR ART

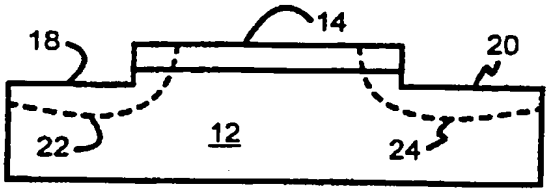


FIGURE 2

PRIOR ART

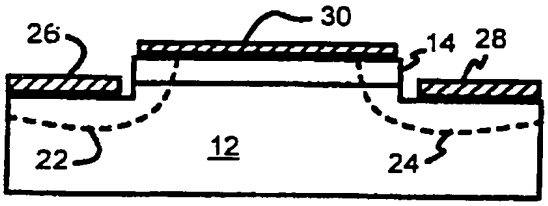


FIGURE 3

PRIOR ART

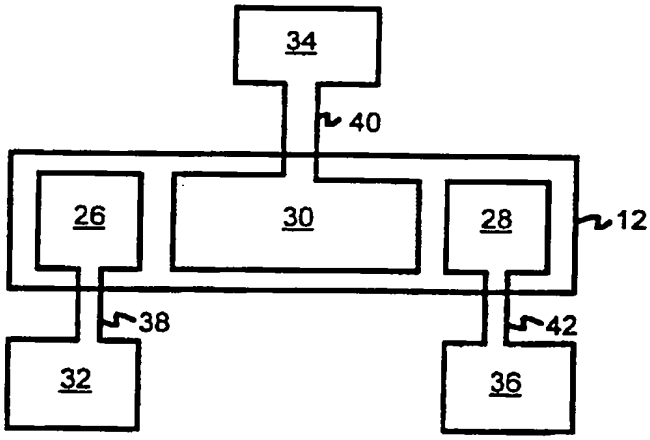
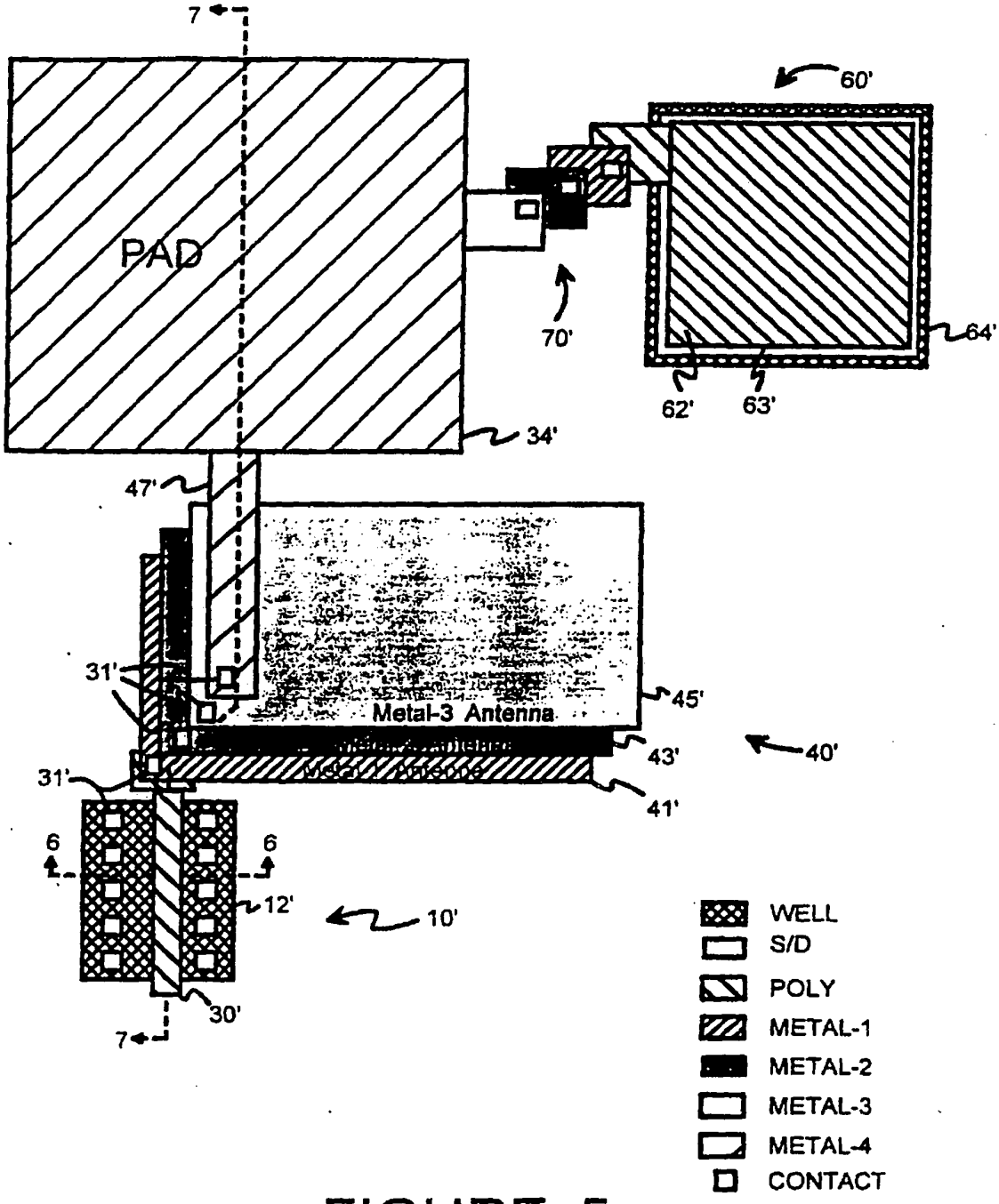


FIGURE 4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PAD
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Metal-3 Antenna
45'
43'
40'
31'
41'
6
6
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7
WELL
S/D
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METAL-1
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METAL-3
METAL-4
CONTACT

FIGURE 5

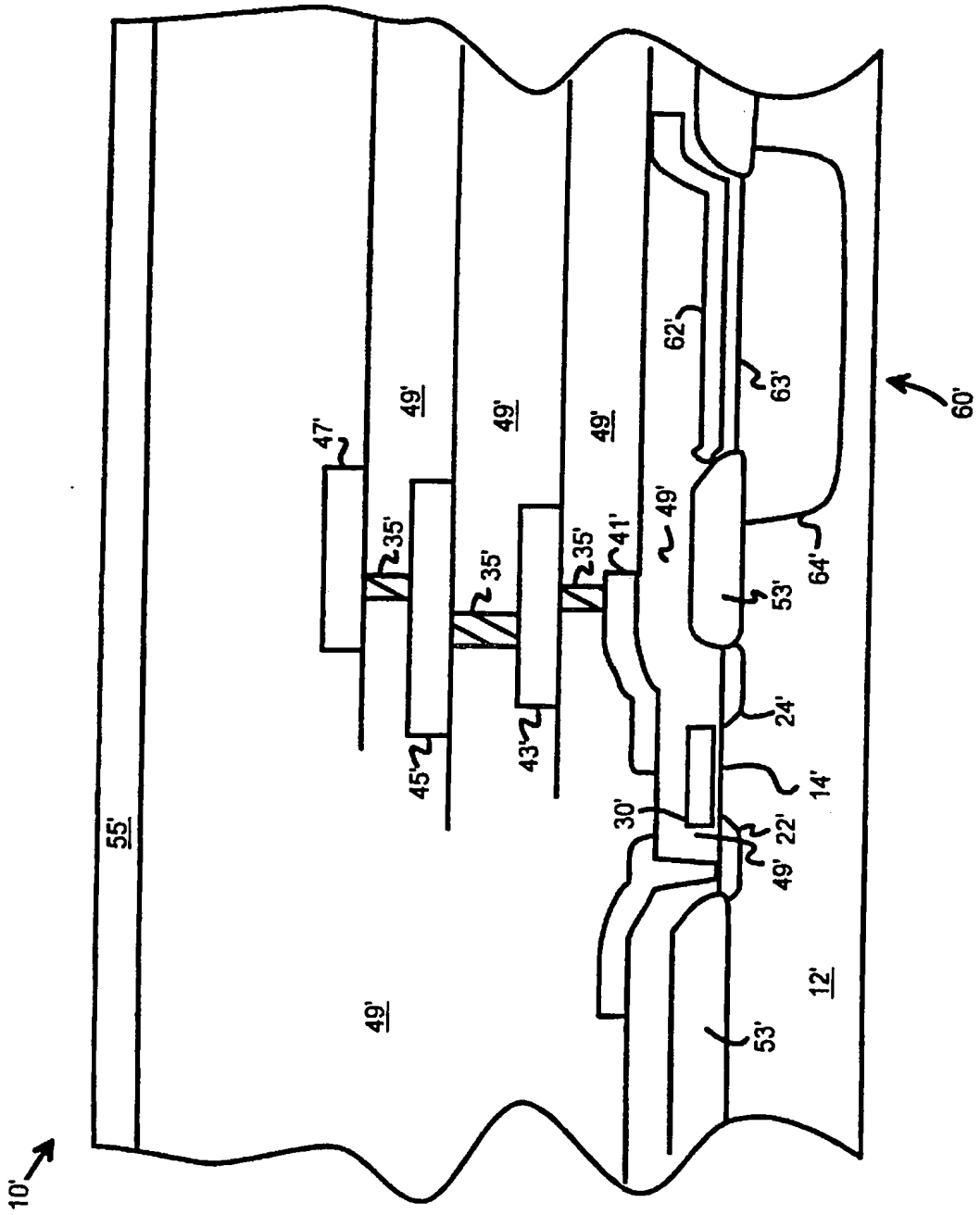
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FIGURE 6

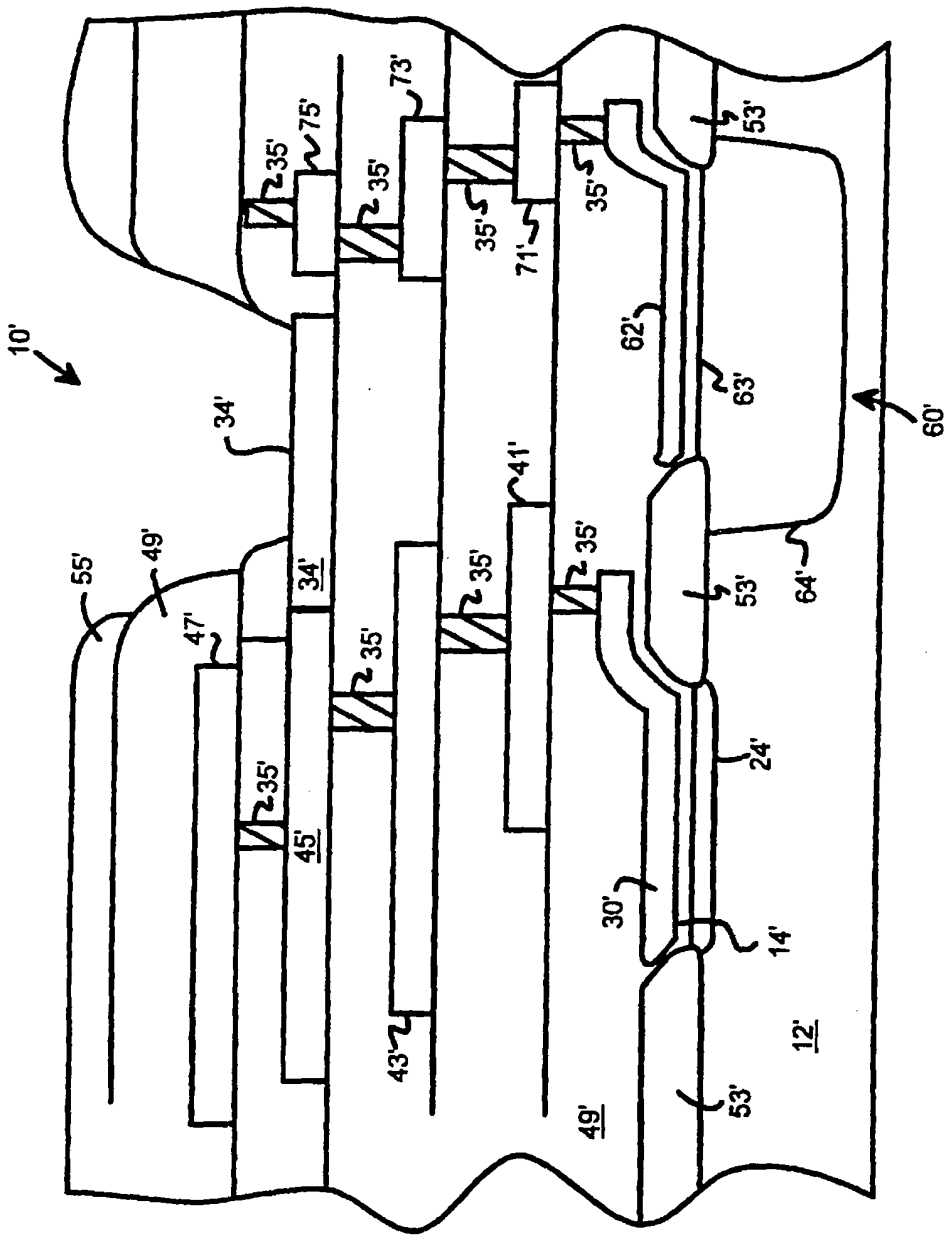

FIGURE 7

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 95/14284

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 350 710 (HONG GARY ET AL) 27 September 1994 see claim 1; figure 1 ---	1
A	EP,A,0 166 112 (SONY CORP) 2 January 1986 see claims 1,16 ---	1
	EP,A,0 076 006 (PHILIPS NV) 6 April 1983 see page 6, line 16 - line 22; claim 1; figure 1 ---	1
A	PATENT ABSTRACTS OF JAPAN vol. 016 no. 259 (E-1215) ,11 June 1992 & JP,A,04 057343 (SONY CORP) 25 February 1992, see abstract ---	1
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

Inter nal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 631 571 (TSUBOKURA FUSAO) 23 December 1986	

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter nal Application No
PCT/US 95/14284

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-5350710	27-09-94	NONE		
EP-A-0166112	02-01-86	JP-A-	60231369	16-11-85
		JP-A-	60231370	16-11-85
		US-A-	4982247	01-01-91
EP-A-0076006	06-04-83	NL-A-	8104414	18-04-83
		CA-A-	1186419	30-04-85
		JP-A-	58067071	21-04-83
		US-A-	4546371	08-10-85
US-A-4631571	23-12-86	JP-C-	1644132	28-02-92
		JP-B-	3007142	31-01-91
		JP-A-	59167049	20-09-84